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POWER EFFICIENT TEST PATTERN GENERATION SCHEME FOR BUILT-IN-SELF-TEST USING LFSR

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ABSTRACT

Functional broadside tests are two-pattern scan based tests that avoid over testing by ensuring that a circuit traverses only reachable states during the functional clock cycles of a test. These consist of the input vectors and the respective responses. They check for perfect operation of a verified design by testing the internal chip nodes. the Functional tests cover a very high percentage of modeled faults in logic circuits and their generation is the main topic of this paper. These functional vectors are generated from the Test pattern generation scheme especially using LFSR due to internal architecture of LFSR Scheme repeated patterns are generated using the proposed scheme these test patterns are avoided and circuits are efficiently verified without any power losses. Any vectors applied are understood to be functional fault coverage vectors applied during manufacturing test. If the patterns of the input test vector results a fault simulation, then circuit test is going to fail. This paper shows the on chip test Generation for a bench mark circuit using simple fixed hardware design with small number of parameters altered in the design for the generation of no of patterns.

KEYWORDS: Power Efficient Test Pattern Generation Scheme